

General Description

The MY34N20F is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

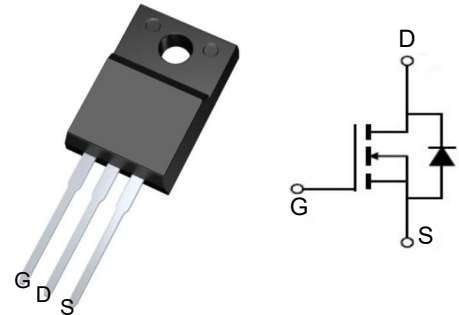


Features

V_{DSS}	200	V
I_D	34	A
P_D ($T_C = 25^\circ\text{C}$)	158	W
$R_{DS(ON)}$ (at $V_{GS} = 10\text{V}$)	60	$\text{m}\Omega$

Application

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY34N20F	TO-220F	MY34N20F	1000

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current -continuous	40	A
I_{DM}	Drain Current -pulse	112	A
V_{GSS}	Gate-Source Voltage	± 30	V
EAS	Single Pulsed Avalanche Energy	588	mJ
IAR	Avalanche Current	28	A
EAR	Repetitive Avalanche Current	15.8	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5	V/ns
P_D $T_C = 25^\circ\text{C}$	Power Dissipation	158	W
T_J, T_{STG}	Operating and Storage Temperature Range	$-55 \sim +150$	$^\circ\text{C}$
TL	Maximum Lead Temperature for Soldering Purposes	300	$^\circ\text{C}$
$R_{th(j-c)}$	Thermal Resistance, Junction to Case	0.79	$^\circ\text{C/W}$
$R_{th(j-A)}$	Thermal Resistance, Junction to Ambient	62.5	$^\circ\text{C/W}$

Electrical Characteristics ($T_C=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Tests conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	200	-	-	V
$IDSS$	Zero Gate Voltage Drain Current	$V_{DS}=200\text{V}$, $V_{GS}=0\text{V}$, $T_C=25^{\circ}\text{C}$	-	-	1	μA
$IGSSF$	Gate-body leakage current, forward	$V_{DS}=0\text{V}$, $V_{GS}=30\text{V}$	-	-	100	nA
$IGSSR$	Gate-body leakage current, reverse	$V_{DS}=0\text{V}$, $V_{GS}=-30\text{V}$	-	-	-100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=14.0\text{A}$	-	60	75	m Ω
g_{fs}	Forward Transconductance	$V_{DS}=40\text{V}$, $I_D=14.0\text{A}$	-	25	-	S
C_{iss}	Input capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	2400	-	pF
C_{oss}	Output capacitance		-	430	-	pF
C_{rss}	Reverse transfer capacitance		-	55	-	pF
$t_{d(on)}$	Turn-On delay time	$V_{DD}=100\text{V}$, $I_D=34\text{A}$, $R_G=25\Omega$ $V_{GS}=10\text{V}$	-	40	-	ns
t_r	Turn-On rise time		-	280	-	ns
$t_{d(off)}$	Turn-Off delay time		-	125	-	ns
t_f	Turn-Off Fall time		-	115	-	ns
Q_g	Total Gate Charge	$V_{DS}=160\text{V}$, $I_D=34\text{A}$ $V_{GS}=10\text{V}$	-	60	-	nC
Q_{gs}	Gate-Source charge		-	17	-	nC
Q_{gd}	Gate-Drain charge		-	27	-	nC
I_S	Continuous Body Diode Current	$T_C=25\text{ }^{\circ}\text{C}$	-	-	31	A
I_{SM}	Pulsed Diode Forward Current		-	-	124	A
V_{SD}	Body Diode Voltage	$V_{GS}=0\text{V}$, $I_S=34\text{A}$	-		1.4	V
t_{rr}	Reverse recovery time	$V_{GS}=0\text{V}$, $I_S=34\text{A}$ $dI_F/dt=100\text{A}/\mu\text{s}$		150		ns
Q_{rr}	Reverse recovery charge			0.95		μC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . $L=0.1\text{mH}$, $I_{AS}=34\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
- 3、The test condition is Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and IDM , in real applications , should be limited by total power dissipation.

Electrical Characteristics

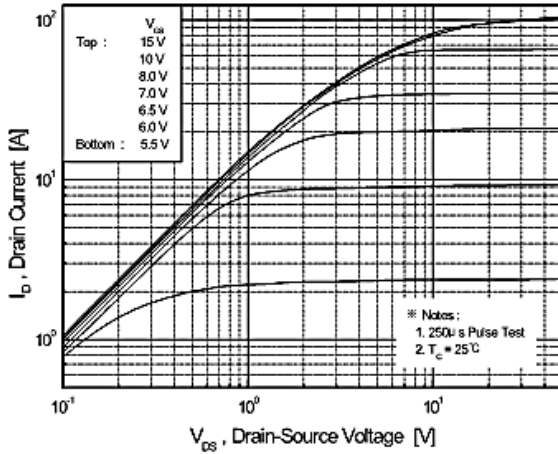


Figure 1. On-Region Characteristics

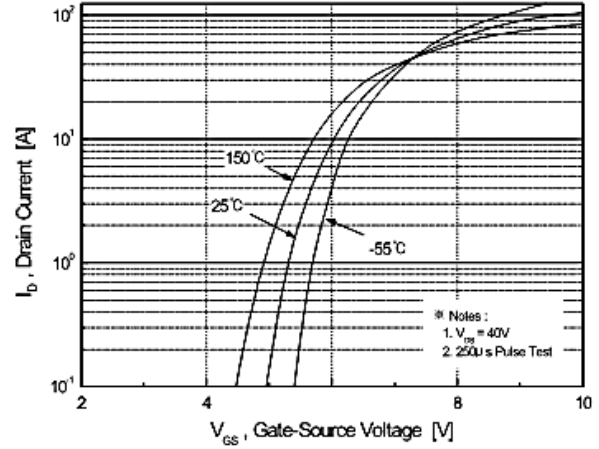


Figure 2. Transfer Characteristics

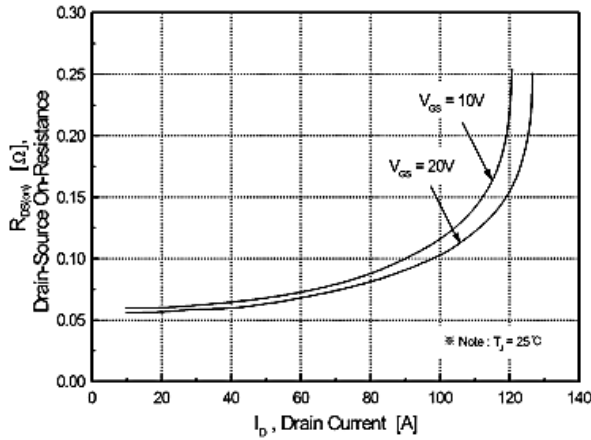


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

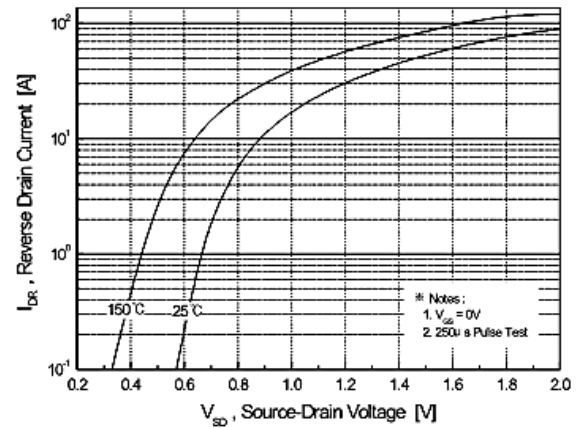


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

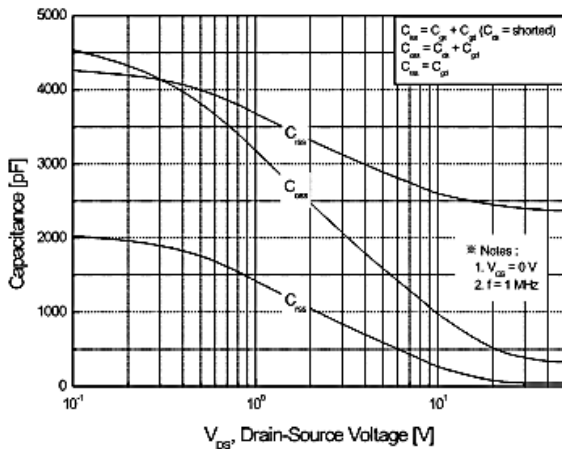


Figure 5. Capacitance Characteristics

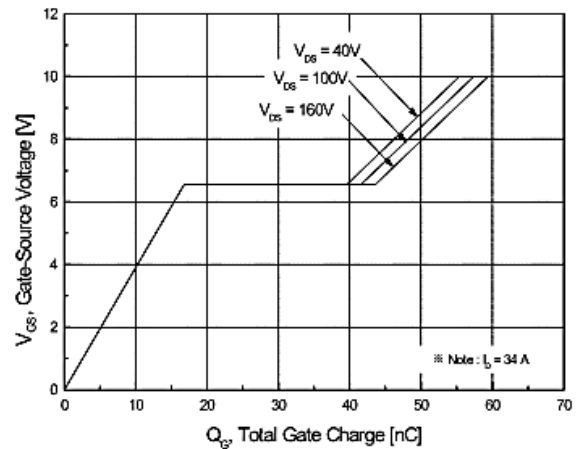


Figure 6. Gate Charge Characteristics

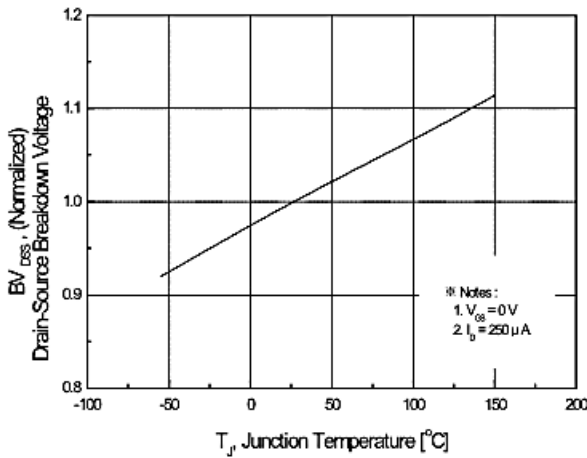


Figure 7. Breakdown Voltage Variation vs. Temperature

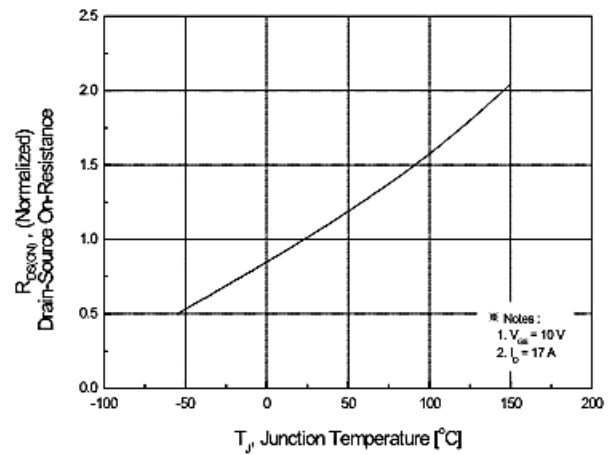


Figure 8. On-Resistance Variation vs. Temperature

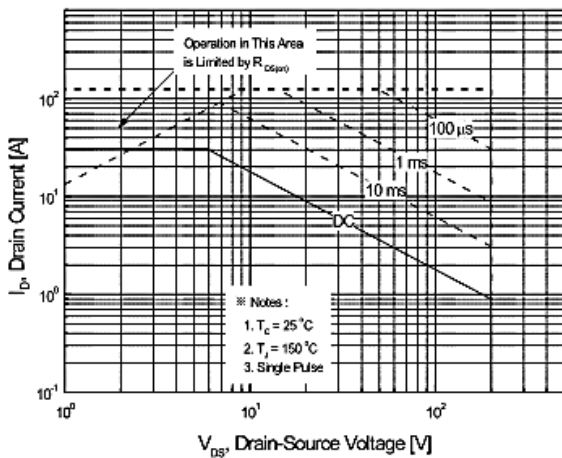


Figure 9. Maximum Safe Operating Area

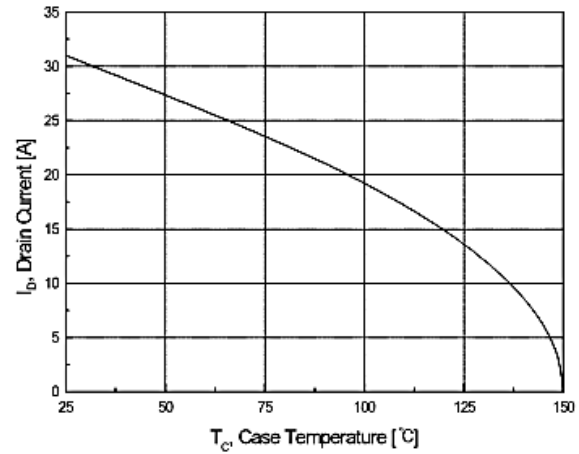


Figure 10. Maximum Drain Current vs. Case Temperature

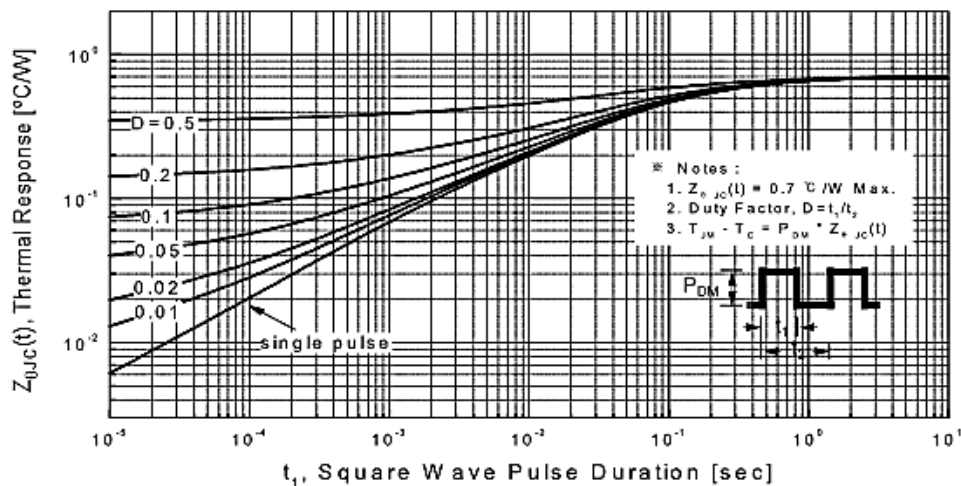
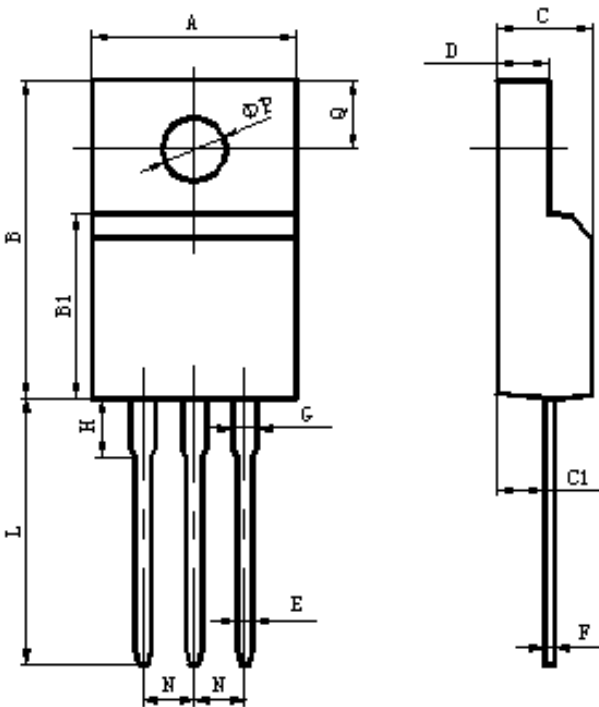


Figure 11. Transient Thermal Response Curve

Package Mechanical Data-TO-220F Single



Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.40	2.90
L*	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
Φ P	2.90	3.30