

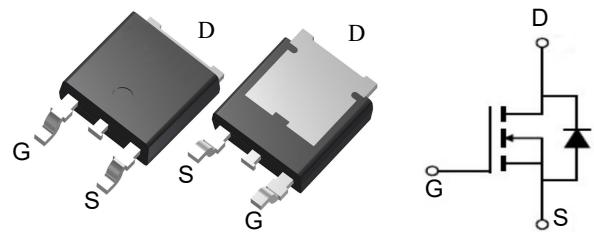
## General Description

The MY6N80D is silicon N-CH Enhanced VDMOSFETs is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



## Features

V <sub>DSS</sub>	800	V
I <sub>D</sub>	6	A
P <sub>D</sub> (T <sub>C</sub> =25°C)	125	W
R <sub>DS(ON)</sub> (at V <sub>GS</sub> =4.5V)	740	mΩ



## Application

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)
- Switch Mode Power Supply (SMPS)

## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY6N80D	TO-252-2L	MY6N80D	2500

## Absolute Maximum Ratings (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V <sub>GS</sub> = 0V)	V <sub>DS</sub>	800	V
Continuous Drain Current	I <sub>D</sub>	6	A
Pulsed Drain Current (note1)	I <sub>DM</sub>	18	A
Gate Source Voltage	V <sub>GS</sub>	±30	V
Single Pulse Avalanche Energy (note2)	E <sub>AS</sub>	198	mJ
Avalanche Current (note1)	I <sub>AR</sub>	3.5	A
Repetitive Avalanche Energy (note1)	E <sub>AR</sub>	14	mJ
Power Dissipation (T <sub>c</sub> = 25°C)	P <sub>D</sub>	125	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C
Thermal Resistance, Junction-to-Case	R <sub>thJC</sub>	1.0	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>thJA</sub>	62	°C/W

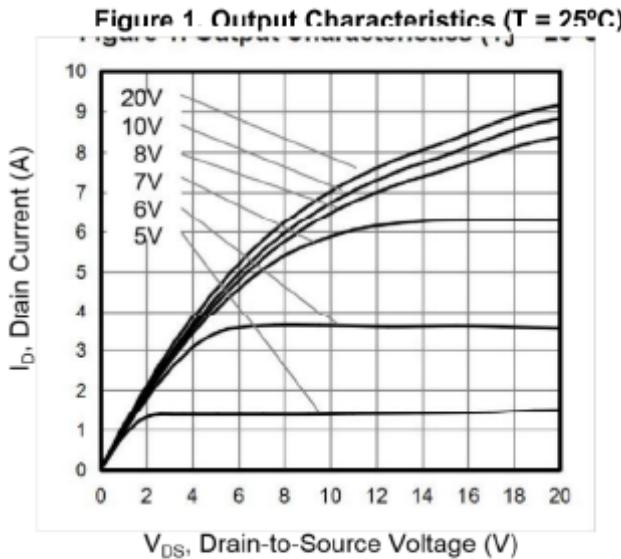
**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min.	Type	Max	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	800	--	--	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 800V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C	--	--	1	μA
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V	--	--	±100	nA
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.5	--	4.5	V
Drain-Source On-Resistance (Note3)	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 4.0A	--	740	830	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz	--	611	--	pF
Output Capacitance	C <sub>oss</sub>		--	18	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	0.9	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 520V, I <sub>D</sub> = 4.0A, V <sub>GS</sub> = 10V	--	17.7	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	2.8	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	6.1	--	
Turn-on Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> = 400V, I <sub>D</sub> = 4.0A, R <sub>G</sub> = 25 Ω	--	10	--	ns
Turn-on Rise Time	T <sub>r</sub>		--	33	--	
Turn-off Delay Time	T <sub>d(off)</sub>		--	30	--	
Turn-off Fall Time	T <sub>f</sub>		--	28	--	
Continuous Body Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	--	--	6	A
Pulsed Diode Forward Current	I <sub>SM</sub>		--	--	18	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25°C, I <sub>SD</sub> = 4.0A, V <sub>GS</sub> = 0V	--	--	1.4	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 4.0A, dI <sub>F</sub> /dt = 100A /μs	--	248	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	2.4	--	

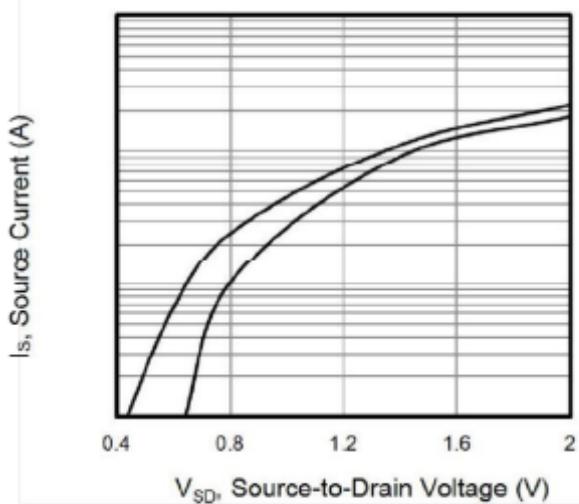
**Notes**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 4A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25 °C
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

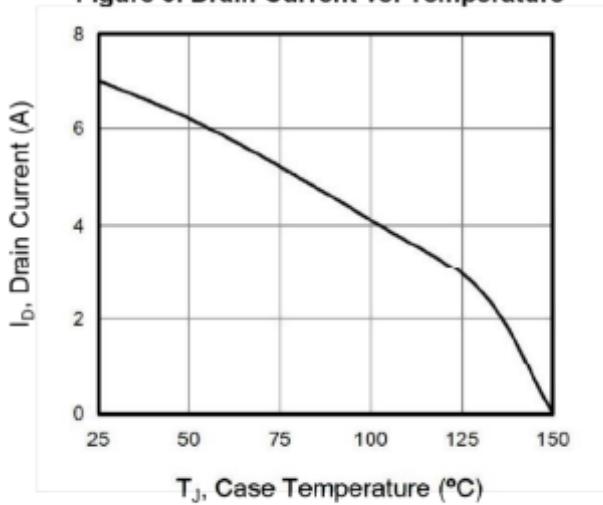
### Typical Characteristics



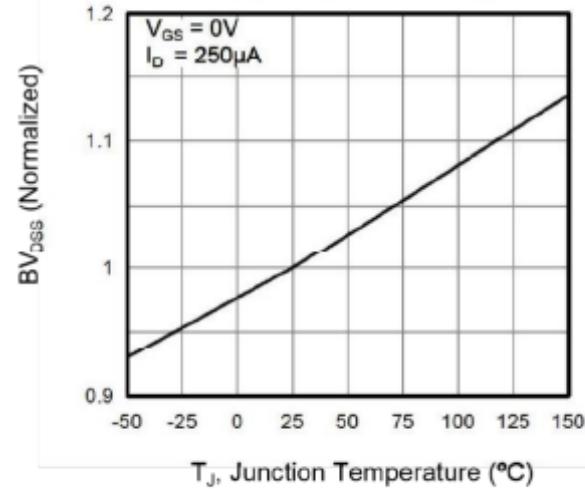
**Figure 2. Body Diode Forward Voltage**



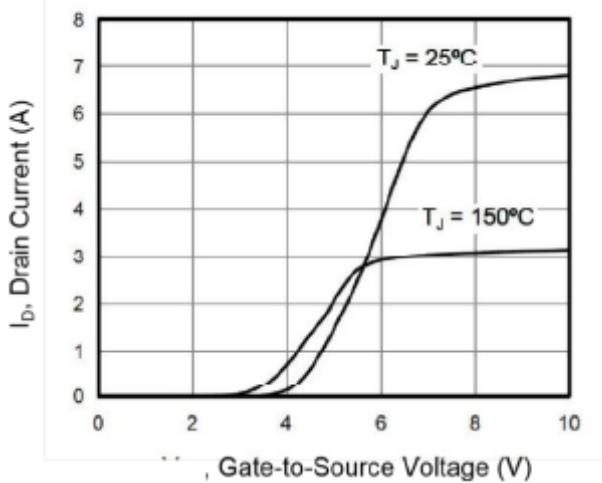
**Figure 3. Drain Current vs. Temperature**



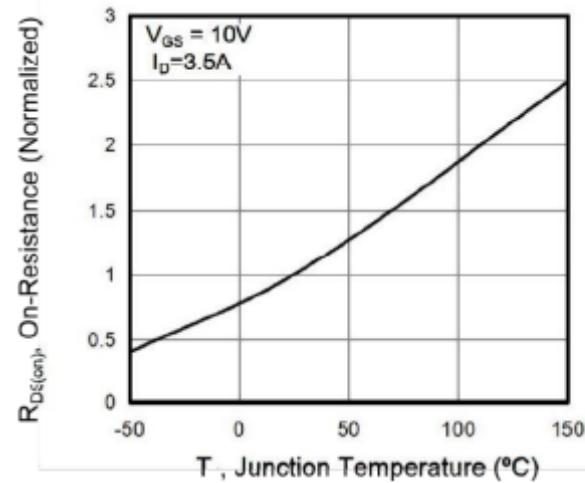
**Figure 4.  $\text{BV}_{\text{DSS}}$  Variation vs. Temperature**

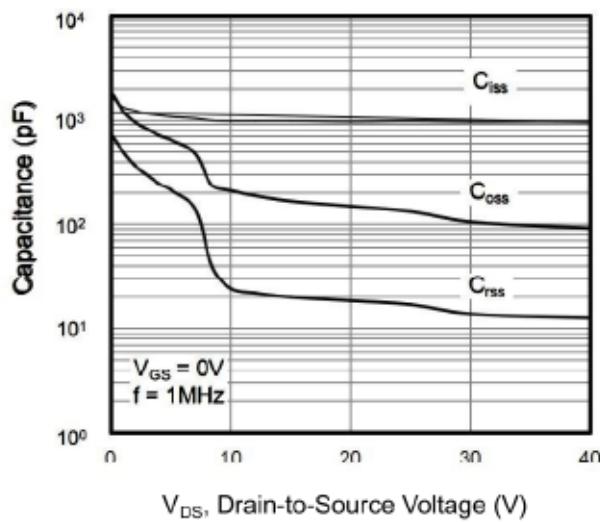
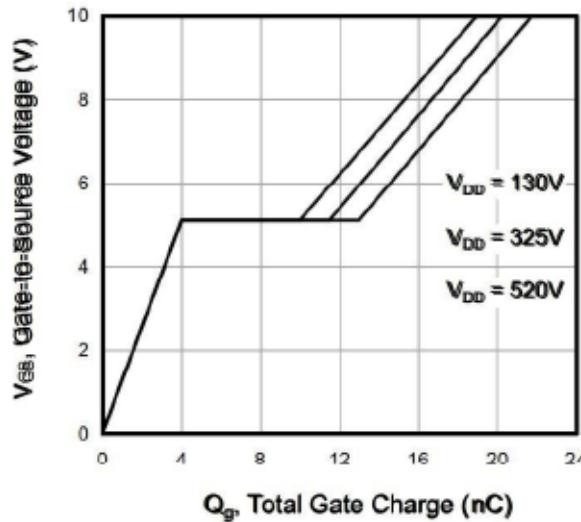
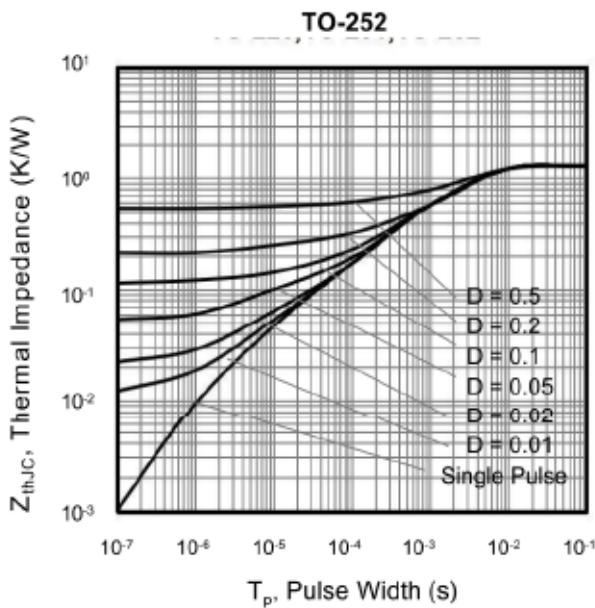
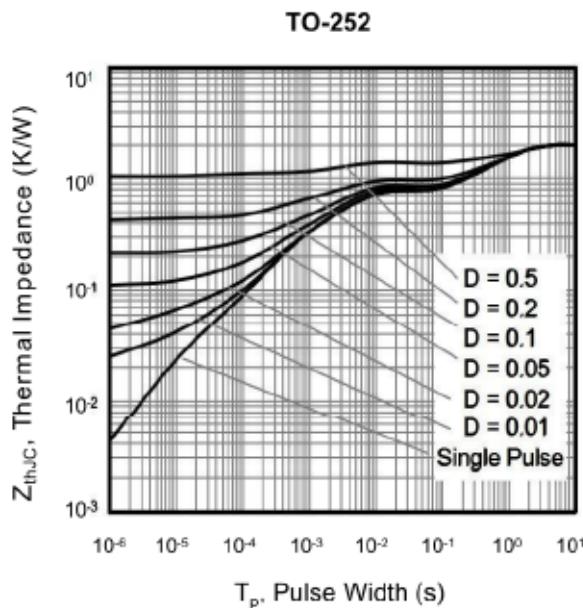


**Figure 5. Transfer Characteristics**



**Figure 6. On-Resistance vs. Temperature**



**Figure 7. Capacitance****Figure 8. Gate Charge****Figure 9. Transient Thermal Impedance****Figure 10. Transient Thermal Impedance****Figure A: Gate Charge Test Circuit and Waveform**

