

## General Description

The MY7N60D is silicon N-channel Enhanced VDMOSFETS, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

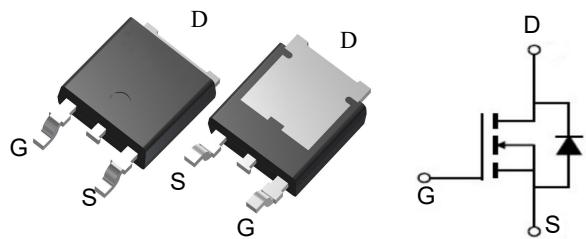


## Features

V <sub>DSS</sub>	600	V
I <sub>D</sub>	7	A
P <sub>D</sub> ( T <sub>C</sub> = 25 °C)	39	W
R <sub>DS(ON)</sub> (at V <sub>GS</sub> = 10V)	1.2	Ω

## Application

- High efficiency switch mode power supplies
- Power factor correction
- Electronic lamp ballast



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY7N60D	TO-252	MY7N60D	2500

## Absolute Maximum Ratings (T<sub>c</sub>=25 °C unless otherwise noted)

Symbol	Parameters	Ratings	Unit
V <sub>DSS</sub>	Drain-Source Voltage	600	V
V <sub>GS</sub>	Gate-Source Voltage-Continuous	±30	V
I <sub>D</sub>	Drain Current-Continuous (Note 2)	7	A
I <sub>DM</sub>	Drain Current-Single Plused (Note 1)	28	A
P <sub>D</sub>	Power Dissipation (Note 2)	39	W
T <sub>j</sub>	Max.Operating junction temperature	150	°C/W

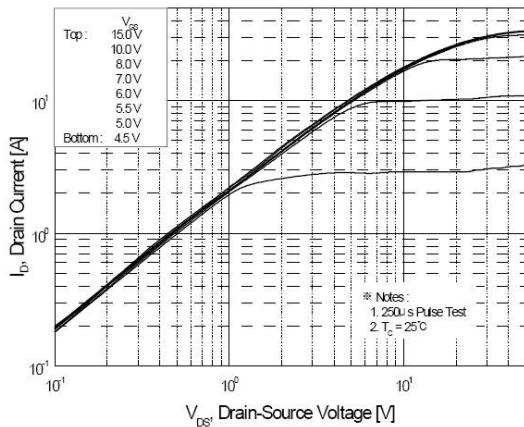
**Electrical Characteristics (T<sub>c</sub>=25 °C, unless otherwise noted)**

Symbol	Parameters	Min	Typ	Max	Units	Conditions
<b>Static Characteristics</b>						
B <sub>VDSS</sub>	Drain-Source Breakdown VoltageCurrent (Note 1)	600	--	--	mA	I <sub>D</sub> =250μA V <sub>GS</sub> =0V , T <sub>J</sub> =25°C
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	--	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
R <sub>DS(on)</sub>	Drain-Source On-Resistance	--	1.2	1.4	Ω	V <sub>GS</sub> =10V , I <sub>D</sub> =3.5A
I <sub>GSS</sub>	Gate-Body Leakage Current	--	--	±100	nA	V <sub>GS</sub> =±30V , V <sub>DS</sub> =0
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	--	--	1	μA	V <sub>DS</sub> =650V , V <sub>GS</sub> =0
g <sub>fs</sub>	Forward Transconductance	2.3	--	--	S	V <sub>DS</sub> =15V, I <sub>D</sub> =3.5A
<b>Switching Characteristics</b>						
T <sub>d(on)</sub>	Turn-On Delay Time	--	48	80	ns	V <sub>DS</sub> =325V , I <sub>D</sub> =7A, R <sub>G</sub> =25Ω (Note 2)
T <sub>r</sub>	Rise Time	--	135	170	ns	
T <sub>d(off)</sub>	Turn-Off Delay Time	--	135	175	ns	
T <sub>f</sub>	Fall Time	--	280	320	ns	
Q <sub>g</sub>	Total Gate Charge	--	30	65	nC	V <sub>DS</sub> =520, V <sub>GS</sub> =10V , I <sub>D</sub> =7A (Note 2)
Q <sub>gs</sub>	Gate-Source Charge	--	6.5	--	nC	
Q <sub>gd</sub>	Gate-Drain Charge	--	13.5	--	nC	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	--	1080	1690	pF	V <sub>DS</sub> =25V , V <sub>GS</sub> =0, f=1MHz
C <sub>oss</sub>	Output Capacitance	--	118	200	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance	--	30	45	pF	
I <sub>s</sub>	Continuous Drain-Source Diode Forward Current (Note 2)	--	--	7	A	
V <sub>SD</sub>	Diode Forward On-Voltage	--	--	1.4	V	I <sub>s</sub> =7A , V <sub>GS</sub> =0
R <sub>th(j-c)</sub>	Thermal Resistance, Junction to Case	--	--	2.6	°C/W	

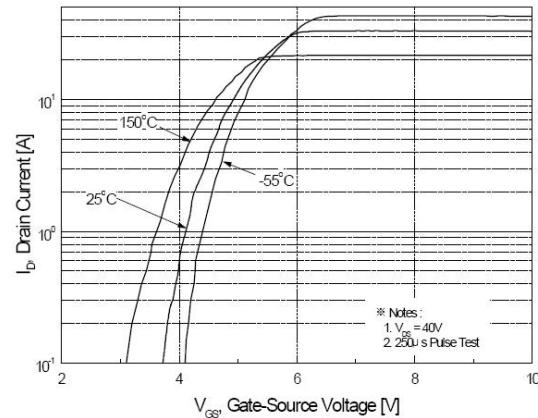
Note 1: Repetitive Rating : Pulse width limited by maximum junction temperature

Note 2: Pulse test: PW &lt;= 300us , duty cycle &lt;= 2%.

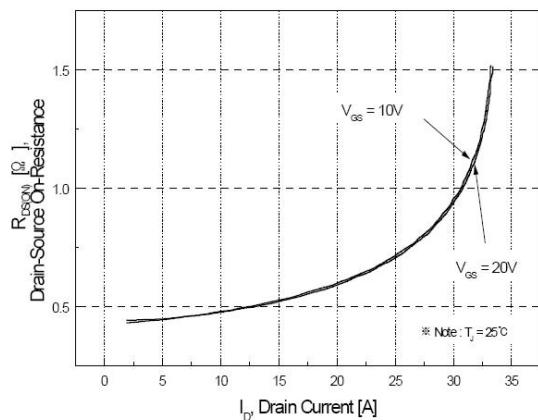
### Ratings and Characteristic curves



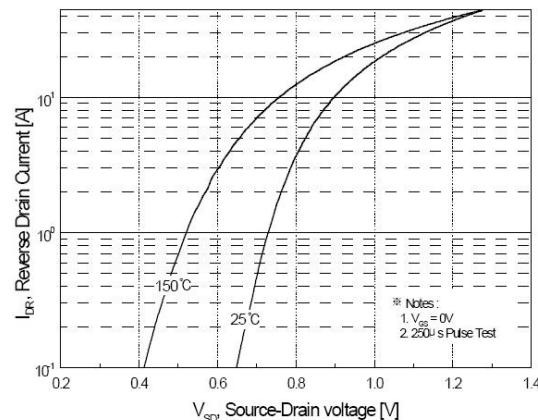
**Figure 1. On-Region Characteristics**



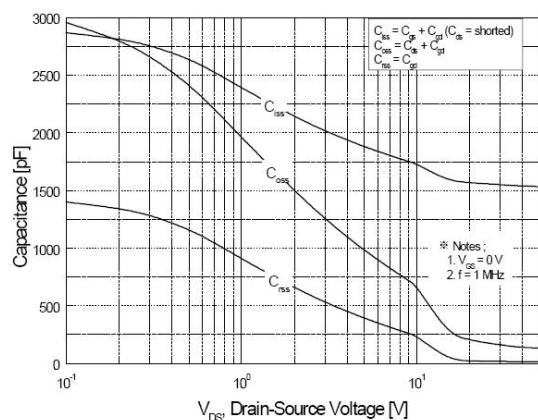
**Figure 2. Transfer Characteristics**



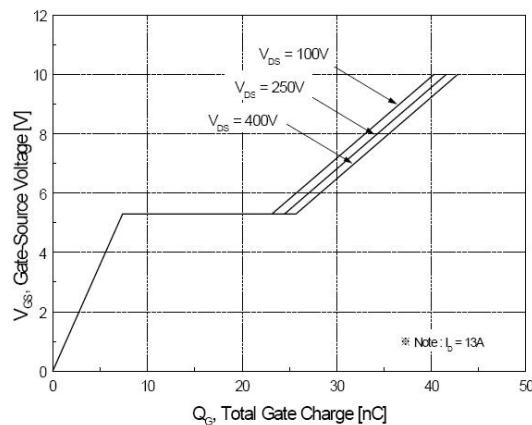
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



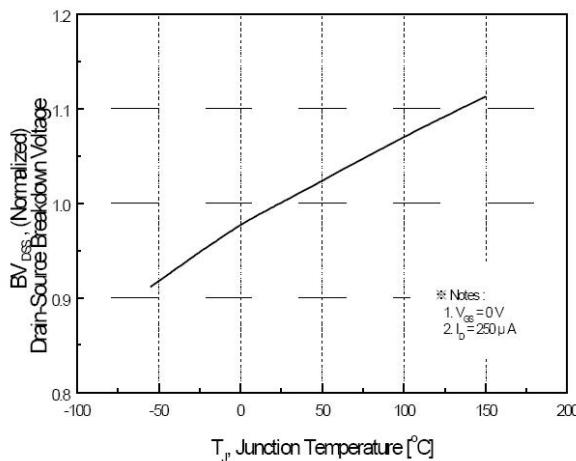
**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**



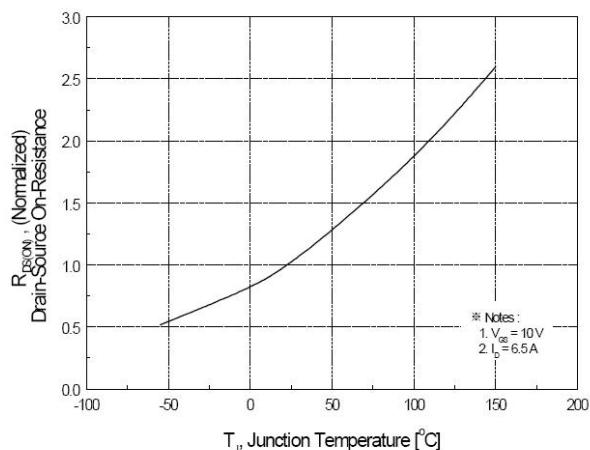
**Figure 5. Capacitance Characteristics**



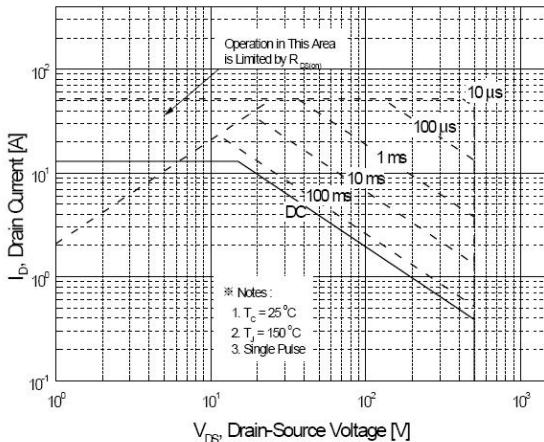
**Figure 6. Gate Charge Characteristics**



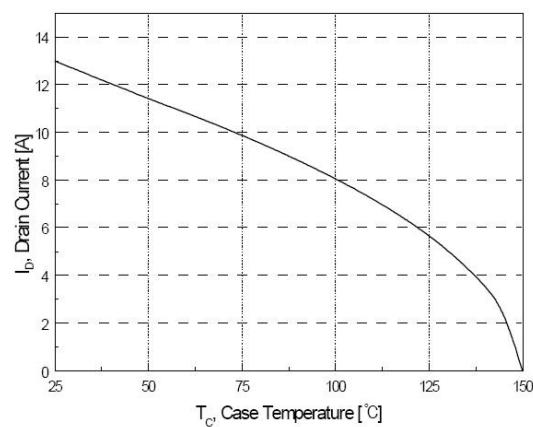
**Figure 7. Breakdown Voltage Variation  
vs Temperature**



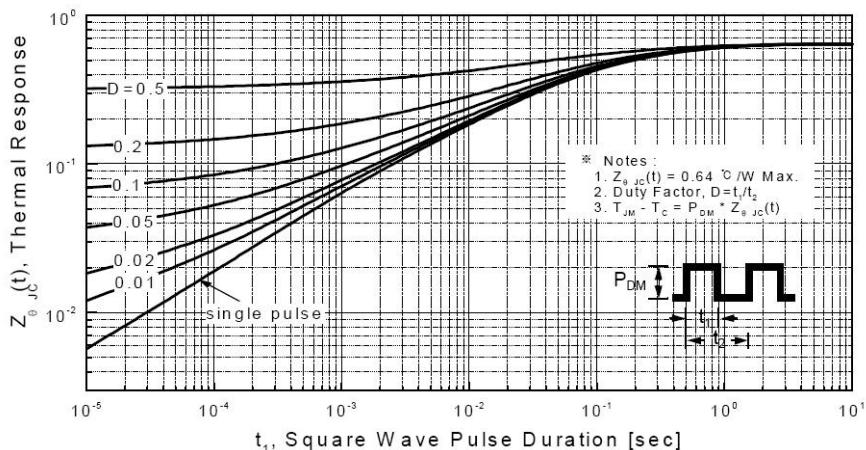
**Figure 8. On-Resistance Variation  
vs Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current  
vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

Fig 12. Gate Charge Test Circuit &amp; Waveform

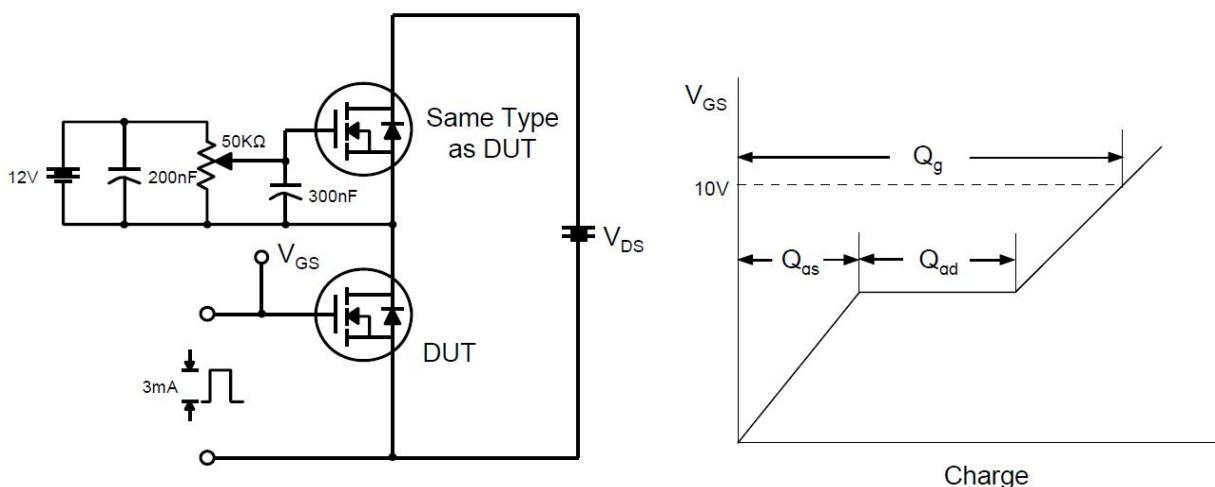


Fig 13. Resistive Switching Test Circuit &amp; Waveforms

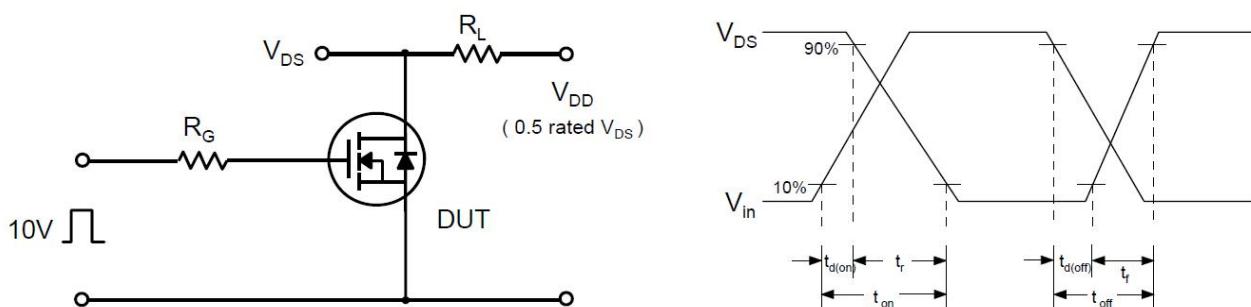


Fig 14. Unclamped Inductive Switching Test Circuit &amp; Waveforms

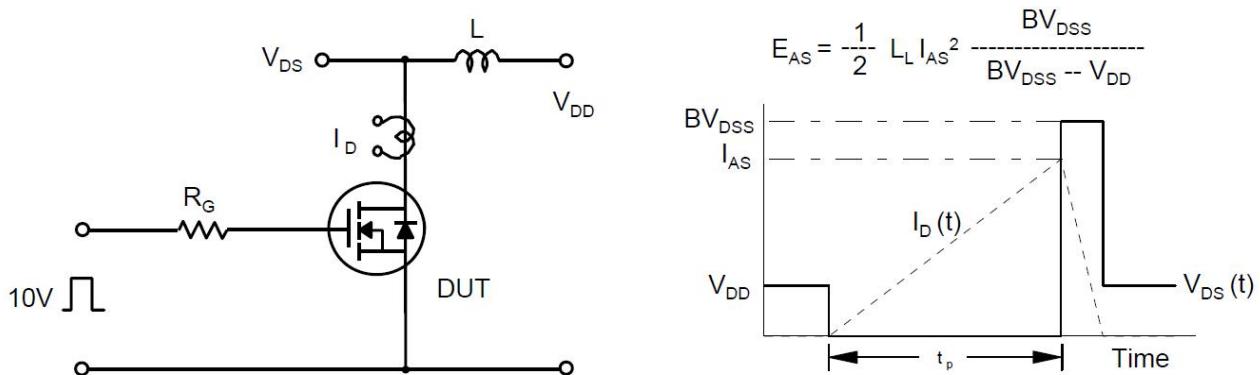
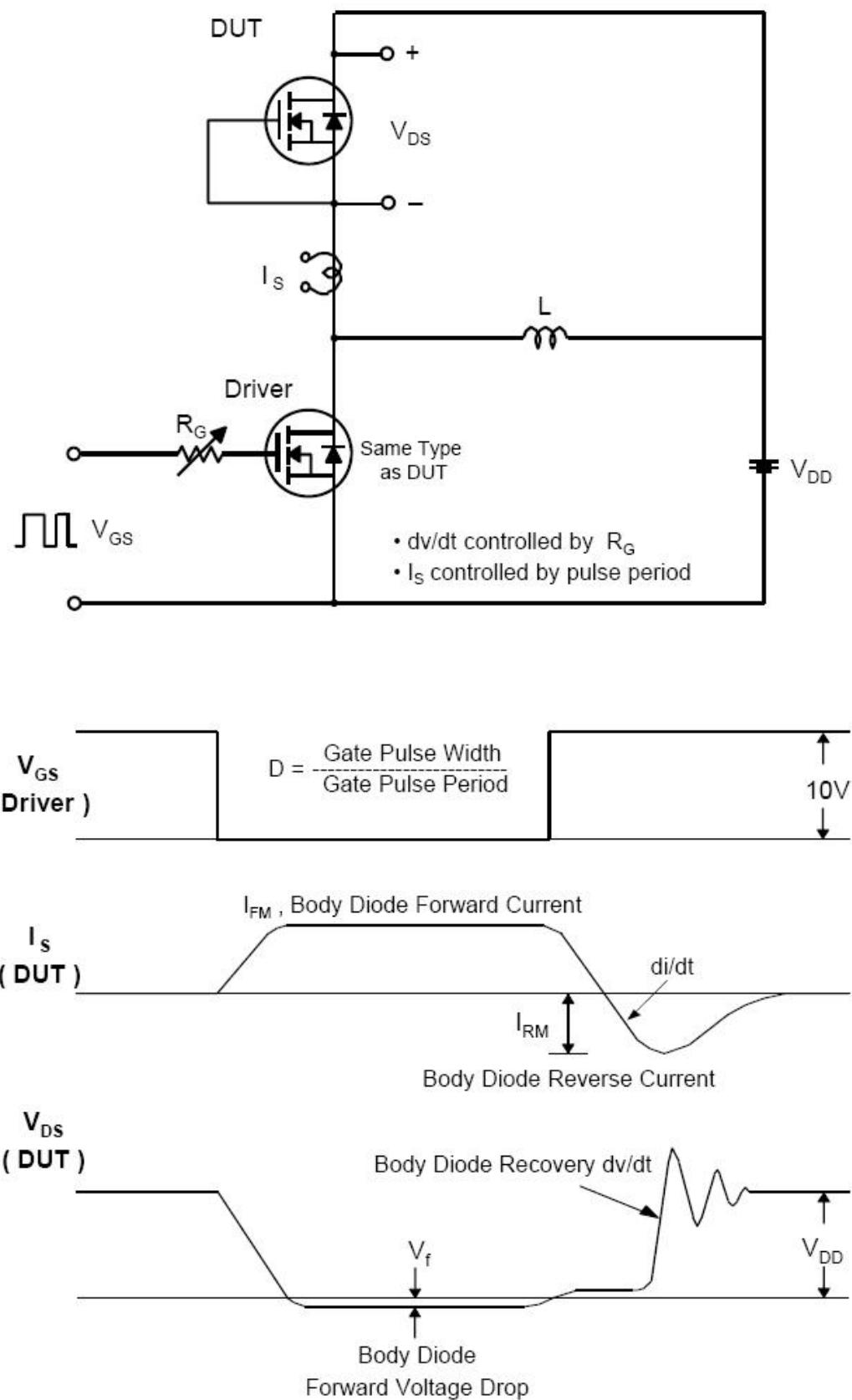
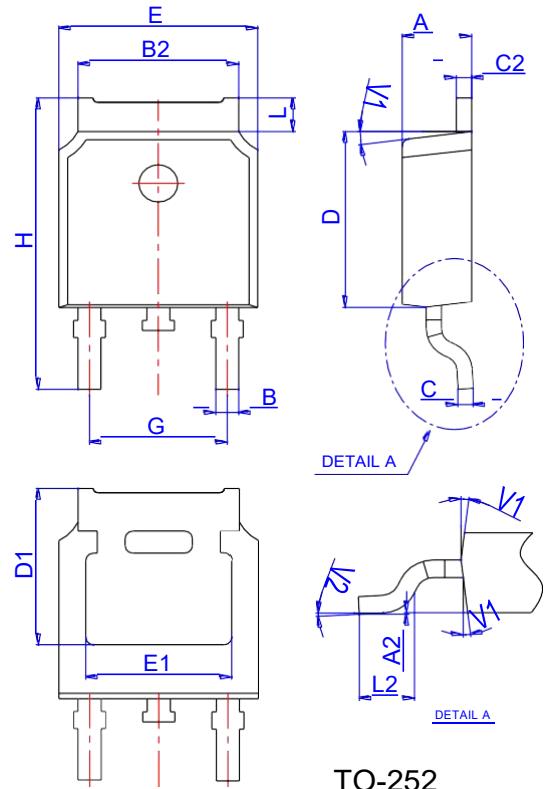
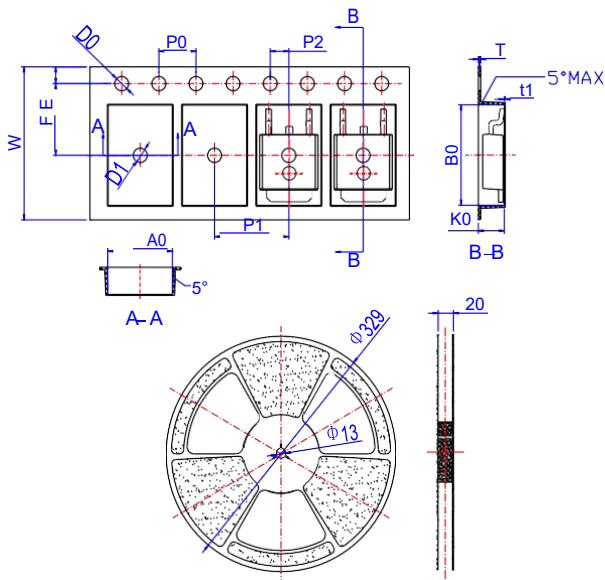


Fig 15. Peak Diode Recovery dv/dt Test Circuit &amp; Waveforms



**Package Mechanical Data-TO-252-JQ Single**


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10			2.50	0.083	
A2	0			0.10	0	
B	0.66			0.86	0.026	
B2	5.18			5.48	0.202	
C	0.40			0.60	0.016	
C2	0.44			0.58	0.017	
D	5.90			6.30	0.232	
D1	5.30REF			0.209REF		
E	6.40			6.80	0.252	
E1	4.63				0.182	
G	4.47			4.67	0.176	
H	9.50			10.70	0.374	
L	1.09			1.21	0.043	
L2	1.35			1.65	0.053	
V1		7°				7°
V2	0°			6°	0°	
						6°

**Reel Specification-TO-252**


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24			0.027	0.009	
t1	0.10				0.004	
10P0	39.80	40.00	40.20	1.567	1.575	1.583